What is claimed is:

1. A sampling clock generator circuit comprising: a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3; a delay line including series-connected 2m or 2m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock signal; and a PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line, a voltage of said second power supply line being set substantially equal to the voltage of said first power supply line and the delayed clock obtained by said second inverters is used as a sampling clock.

2. A sampling clock generator circuit as claimed in claim 1, wherein said first and second power supply lines are directly connected each other and set to substantially an equal voltage, the delayed clocks obtained from said second inverters are used to convert a serially transmitted data into a parallel data.

3. A sampling clock generator circuit as claimed in claim 2, wherein said ring oscillator generates pulses having period substantially equal to a period of the external clock signal and said PLL circuit includes a phase comparator circuit for comparing the phase of the external clock with the phase of the pulses.

4. A sampling clock generator circuit as claimed in claim 3, wherein said external clock signal is transmitted together with the data transmitted serially

through a line different from that of the data transmitted serially and the data is serially transmitted at a frequency n times that of the transmitted clock in units of n data, where n is an integer equal to or larger than 2.

5. A sampling clock generator circuit as claimed in claim 4, wherein m is 7 and the external clock signal is serially transmitted from a computer together with the data.

6. A sampling clock generator circuit comprising: a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3; a delay line including series-connected 2m or 2m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock; a first PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line, a second PLL circuit for generating a control voltage for locking the clocks outputted said inverters of said delay line by comparing the phase of the external clock with the phase of the clocks outputted from said delay line; and a voltage setting circuit for setting the voltage of said second power supply line on the basis of the voltage of said first power supply line and the control voltage, the delayed clock obtained from said second inverters is used as a sampling clock.

7. A sampling clock generator circuit as claimed in

claim 6, wherein said ring oscillator generates pulses having period substantially equal to a period of the external clock signal, said first PLL circuit includes a first phase comparator circuit for comparing the phase of the external clock signal with the phase of the pulses and said second PLL circuit includes a second phase comparator circuit for comparing the phase of the external clock signal with the phase of the clocks outputted the 2m-th stage inverter of said delay line.

8. A sampling clock generator circuit as claimed in claim 7, wherein said external clock signal is transmitted together with the data transmitted serially through a line different from that of the data transmitted serially and the data is serially transmitted at a frequency n times that of the transmitted clock signal in units of n data, where n is an integer equal to or larger than 2.

9. A sampling clock generator circuit as claimed in claim 8, wherein m is equal to n, said first PLL circuit includes a first charge pump circuit, a first low-pass filter and a first voltage follower, said first charge pump circuit receives the output of the first phase comparator, an output of the first charge pump circuit is inputted to the first low-pass filter, an output of the first low-pass filter is inputted to the first voltage follower, the output of the first voltage follower is connected to said first power supply line, the said second PLL circuit includes a second charge pump circuit, a second low-pass filter and a second voltage follower, said second charge pump circuit

receives the output of the second phase comparator, an output of the second charge pump circuit is inputted to the second low-pass filter, an output of the second low-pass filter is inputted to the second voltage follower and said voltage setting circuit is a synthesizing circuit which synthesizes a voltage signal of the first voltage follower with a voltage of the second voltage follower.

10. A data receiving device comprising: a ring oscillator including series-connected m first inverters connected to a first power supply line, where m is an odd number equal to or larger than 3; a delay line including series-connected 2m or 2m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock and outputting the thus delayed external clock from said second inverters; a PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line; and a serial/parallel converter circuit for converting the transmitted serial data into a parallel data in units of n data, sad serial/parallel converter circuit being supplied with the delayed clock obtained from said second inverters by setting the voltage of said second power supply line substantially equal to the voltage of said first power supply line.

11. A data receiving device comprising: a ring oscillator including series-connected m first inverters connected to a first power supply line, where

m is an odd number equal to or larger than 3; a delay line including series-connected 2m or 2m-1 second inverters connected to a second power supply line, for delaying an externally supplied clock and outputting the thus delayed external clock from said second inverters; a first PLL circuit including a voltage controlled oscillation circuit for controlling an oscillation frequency of said ring oscillator by controlling a voltage of said first power supply line; a second PLL circuit for comparing a phase of the external clock with a phase of the clock outputted from said inverters of said delay line and generating a control voltage for locking the clock outputted from said inverters of said delay line; a voltage setting circuit for setting the voltage of said second power supply line on the basis of the voltage of said first power supply line and the control voltage; and a serial/parallel converter circuit for converting the transmitted serial data into a parallel data in units of n data, said serial/parallel converter circuit being supplied with the delayed clock obtained from said second inverters.

12. A sampling clock generator circuit as claimed in claim 11, wherein said first and second power supply lines are directly connected each other and set to substantially an equal voltage, the delayed clocks obtained from said second inverters are used to convert a serially transmitted data into a parallel data.